F1C800 Datasheet

HD Video Boombox Processor

Revision 1.0

Mar. 14, 2017

Revision History

Revision	Date	Description
1.0	Mar.14,2017	Initial Release Version.

Declaration

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About This Documentation

The documentation describes features of each module, pin/signal characteristics, current consumption, PLL electrical characteristics, the interface timing, thermal and package of F1C800 processor. The documentation is intended to provide guidance to the hardware designers for electronics or sales personnel for electronic components. This documentation assumes that the reader has a background in electronic components. For details about register descriptions of each module, see the *F1C800 User Manual*.

1. Overview

The F1C800 processor represents Allwinner's latest achievement in HD Video Boombox products. The processor adopts the latest H.265 video decoder, advanced audio system, low-power technology and high integration architecture design. These features help F1C800 keep the leading user experience in HD video playback, image quality and total performance. Integrated 4-lane MIPI DSI display output interface is up to 1080p@60fps. In order to reduce the BOM cost, the F1C800 integrates an internal DDR2 memory. A number of interfaces, such as RGB LCD, LVDS, TVIN, TVOUT, USB, I2S/PCM, UART, SPI, provide the flexible connecting solutions.

2. Features

2.1. CPU

- ARM926-EJS
- Supports 32 KB Instruction cache and 32 KB Data cache

2.2. Memory Subsystem

Boot ROM

- On-chip memory
- Supports system boot from the following device:
  - SD Card
  - SPI Nor Flash
  - SPI Nand Flash
  - USB OTG

SDRAM

- SIP DDR2 memory
- Supports clock frequency up to 400 MHz

SMHC

- Up to 2 SD/MMC Host Controller(SMHC) interfaces
- Compliant with SD physical layer specification V2.0, SDIO card specification V2.0
- 1-bit or 4-bit data bus transfer mode up to 50 MHz in SDR mode
- Supports block size of 1 to 65535 bytes
- Embedded special DMA to do data transfer

2.3. System Peripheral

CCU

- 10 PLLs
- Supports an external 24 MHz crystal oscillator , an external 32.768 kHz crystal oscillator and an on-chip 16 MHz RC oscillator
- Supports clock configuration and clock generated for corresponding modules
- Supports software-controlled clock gating and software-controlled reset for corresponding modules

Timer

- 2 on-chip Timers with interrupt-based operation
- 1 Watchdog to generate reset signal or interrupt

- Two 33-bit Audio/Video Sync(AVS) Counters to synchronize video and audio in the player

High Speed Timer

- 1 High Speed Timer(HSTimer) with 56-bit counter
- 56-bit counter that can be separated to 24-bit high register and 32-bit low register
- Clock source is synchronized with AHB1 clock, and the pre-scale range is from 1 to 16
- More accurate than other timers

RTC

- Time, Calendar
- Counters second, minute, hour, day, week, month and year with leap year generator
- Alarm: general alarm and weekly alarm

INTC

- Controls the nIRQ Processor
- Sixty-four individually maskable interrupt sources
- 4-level interrupt priority setting
- Supports fast forcing

DMA

- Up to 8-channel DMA
- Interrupt generated for each DMA channel
- Flexible data width of 8/16/32/64-bit
- Supports linear and IO address modes
- Programs the DMA burst size
- Supports data transfer types with memory-to-memory, memory-to-peripheral, peripheral-to-memory

PWM

- Up to 7 PWM channels
- Supports single-pulse, long-period and complementary pair output
- Supports capture input
- Supports programming deadzone output
- Build-in the programmable dead-time generator
- Supports three kinds of output waveform: continuous waveform, pulse waveform and complementary pair
- 0% to 100% adjustable duty cycle
- Up to 100 MHz output frequency
- Minimum resolution is 1/65536
- Supports interrupt generation for PWM output and capture input

KEYADC

- Analog to digital converter with 6-bit resolution for key application
- Maximum sampling frequency up to 250 Hz
- Supports general key, hold key and already hold key

- Supports single , normal and continuous work mode

TP

- 12-bit SAR type A/D converter
- 4-wire I/F
- Touch-pressure measurement (Supports programmable threshold)
- Sampling frequency up to 1 MHz
- Single-ended conversion of touch screen inputs and ratiometric conversion of touch screen inputs
- TACQ up to 262ms
- Median and averaging filter to reduce noise
- Pen down detection, with programmable sensitivity
- Supports X, Y change

Crypto Engine(CE)

- Supports AES, DES, 3DES, SHA-1, MD5
- Supports 160-bit hardware PRNG with 175-bit seed
- 128-bit, 192-bit and 256-bit key size for AES
- Supports ECB, CBC ,CTR,CTS modes for AES
- Supports ECB, CBC,CTR modes for DES/3DES
- Supports 32 words RX FIFO and 32 words TX FIFO for high speed application
- Supports CPU mode and DMA mode

Security ID

- On-chip 512-bit EFUSE for chip ID and other applications
- Supports on-line LDO programming

2.4. Display Subsystem

DE2.0

- Output size up to 2048 x 2048
- Supports 1 UI channel and 1 video channel for main display RT-Mixer
- Supports 1 video channel for aux display
- Supports four layers in each overlay channel, and has a independent scaler
- Supports potter-duff compatible blending operation
- Supports input format :YUV422/YUV420/YUV411/ARGB8888/XRGB8888/RGB888/ARGB4444/ARGB1555/ RGB565
- Supports Frame Packing/Top-and-Bottom/Side-by-Side Full/Side-by-Side Half 3D format data
- Supports SmartColor 2.0 for excellent display experience
  - Adaptive edge sharping
  - Adaptive color enhancement
  - Adaptive contrast enhancement and fresh tone rectify
- Supports dual display: LCD + CVBS Out
- Supports writeback and rotation for high efficient dual display
- Supports online/offline de-interlacer

Display Output

- Supports 18-bit RGB interface
  - Up to 1920x1080@60fps
  - Supports dither function
  - Supports Gamma parameter adjusting
- Supports LVDS interface
  - Dual link LVDS mode output up to 1920x1080@60fps
  - Single link LVDS mode output up to 1366x768@60fps
  - Multiplex pin with RGB interface
- Supports 1-ch TV CVBS output
  - Supports NTSC and PAL mode
  - Plug status auto detecting
- Supports 4-lane MIPI DSI output
  - Up to 1080p@60fps
  - Compliance with MIPI DSI v1.01 and MIPI D-PHY v1.00
  - 1/2/3/4 data lane configuration and up to 1Gbps per lane
  - Supports video mode with sync pulse/burst mode
  - Supports pixel format: RGB888, RGB666, RGB666 packed, and RGB565

2.5. Video Engine

Video Decoder

- Supports multi-format video playback, including:
  - H.265 MP/L5.2: 1080p@45fps
  - H.264 BP/MP/HP Level4.2: 1080p@45fps
  - H.263 BP: 1080p@45fps
  - MPEG1 MP/HL: 1080p@45fps
  - MPEG2 MP/HL: 1080p@45fps
  - MPEG4 SP/ASP L5: 1080p@45fps
  - Sorenson Spark: 1080p@45fps
  - VP8 N/A: 1080p@45fps
  - AVS/AVS+ JiZhun: 1080p@45fps
  - xvid N/A: 1080p@45fps
  - WMV9/VC1 SP/MP/AP: 1080p@30fps
  - JPEG: 45MPPS

2.6. Image Subsystem

TVIN

- 2 channels TV CVBS input to 1 channel CVBS decoder
- Supports NTSC and PAL mode
- Supports YUV422, YUV420 format
- With 3D comb filter
- Programmable brightness, contrast, saturation
- 10-bit video ADCs

2.7. Audio Subsystem

Audio Codec

- Two audio digital-to-analog(DAC) channels
  - 100 ± 3 dB SNR@A-weight
  - Supports ADC sample rates from 8 kHz to 192 kHz
- One audio analog-to-digital(ADC) channel
  - 92 ± 3 dB SNR@A-weight
  - Supports ADC sample rates from 8 kHz to 48 kHz
- Supports analog/digital volume control
- Analog low-power loop from analog to analog outputs
- Supports Dynamic Range Controller(DRC) adjusting the DAC playback output
- Supports Dynamic Range Control(DRC) adjusting the ADC recording input
- Three audio inputs:
  - One microphone input
  - One mono line-in input
  - One stereo FMIN input
- One audio output: One stereo headphone output
- Interrupt and DMA support

I2S/PCM

- Compliant with standard Inter-IC sound(I2S) bus specification
- Compliant with left-justified, right-justified, PCM mode, and TDM(Time Division Multiplexing) format
- Supports 8-channel in TDM mode
- Full-duplex synchronous work mode
- Master and slave mode configured
- Clock frequency up to 100 MHz
- Adjustable audio sample resolution from 8-bit to 32-bit
- Supports up to 8 slots which has adjustable width from 8-bit to 32-bit.
- Supports sample rate from 8 kHz to 192 kHz
- Supports 8-bit u-law and 8-bit A-law companded sample
- One 128 x 32-bit width FIFO for data transmit, one 64 x 32-bit width FIFO for data receive
- Supports programmable PCM frame width: 1 BCLK width (short frame) and 2 BCLKs width (long frame)
- Programmable FIFO thresholds
- Interrupt and DMA Support

2.8. External Peripherals

USB

- One USB 2.0 OTG, with integrated USB PHY
- Supports host/device dual-role function
- Complies with USB 2.0 Specification
- Complies with Enhanced Host Controller Interface(EHCI)Specification, Version 1.0, and the Open Host Controller Interface(OHCI) Specification, Version 1.0a for host mode
- Supports High-Speed (HS, 480 Mbit/s),Full-Speed(FS, 12 Mbit/s) and Low-Speed(LS, 1.5 Mbit/s) in host mode
- Supports High-Speed (HS, 480 Mbit/s), Full-Speed (FS, 12 Mbit/s) in device mode
- Up to 8 user-configurable endpoints (Endpoint1, Endpoint2, Endpoint3, Endpoint4) in device mode

TWI

- Up to 3 TWI(Two Wire Interface) controllers
- Supports Standard mode(up to 100 kbit/s) and Fast mode(up to 400 kbit/s)
- Master/slave configurable
- Allows 10-bit addressing transactions
- Perform arbitration and clock synchronization
- Allows operation from a wide range of input clock frequencies

SPI

- Up to 2 SPI controllers, each SPI has one chip select signal
- Full-duplex synchronous serial interface
- Master/slave configurable
- Mode0~3 are supported for both transmit and receive operations
- Two 64 bytes FIFO for SPI-TX and SPI-RX operation
- DMA-based or interrupt-based operation
- Polarity and phase of the chip select(SPI_SS) and SPI_Clock(SPI_SCLK) are configurable
- Supports single and dual IO mode
- Maximum frequency up to 100 MHz

UART

- Up to 3 UART controllers: one UART for CPU debug, two UART for UART applications
- UART0: 2-wire; UART1/2: 4-wire
- Compliant with industry-standard 16450 and 16550 UARTs
- Supports RS232 protocol
- Supports word length from 5 to 8 bits, an optional parity bit and 1,1.5 or 2 stop bits
- Programmable parity(even, odd and no parity)
- 64 bytes transmit and receive data FIFOs
- Supports clock frequency up to 4 Mbit/s

CIR Receiver

- A flexible receiver for IR remote
- Programmable FIFO threshold

SCR

- One SCR(Smart Card Reader) controller
- Supports ISO/IEC 7816-3:1997(E) and EMV2000 (4.0) Specifications
- Supports adjustable clock rate and bit rate
- Configurable automatic byte repetition
- Supports asynchronous half-duplex character transmission and block transmission
- Supports synchronous and any other non-ISO 7816 and non-EMV cards
- Performs functions needed for complete smart card sessions, including:
  - Card activation and deactivation
  - Cold/warm reset
  - Answer to Reset (ATR) response reception
  - Data transfers to and from the card

TSC

- One TSC(Transport Stream Controller)
- One external Synchronous Parallel Interface (SPI) or one external Synchronous Serial Interface (SSI)
- 32 channels PID filter for TSF
- Multiple transport stream packet (188, 192, 204) format support
- SPI and SSI timing parameters are configurable
- Hardware packet synchronous byte error detecting
- Hardware PCR packet detecting
- Configurable SPI transport stream generator for streams in DRAM memory

2.9. Package

- eLQFP128(SIP DDR2), 14 mm x 14 mm

